

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,138,709 B2
APPLICATION NO. : 10/663485
DATED : November 21, 2006
INVENTOR(S) : Takashi Kumamoto

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4

Lines 32-33, "...intermediate substrate 30..." should read ---intermediate substrate blank 30....--.

Line 39, "...substrate blank 30,..." should read ---intermediate substrate blank 30,...--.

Column 5

Line 1, "...intermediate substrate 30..." should read ---intermediate substrate blank 30...--.

Lines 14-15, "...to over lay..." should read ---to overlay...--.

Lines 61-62, "...second carrier substrate 112,..." should read --...second carrier substrate 112',...--.

Column 6

Line 15, "...102" should read ---102--.

Column 7

Lines 26-27, "...microelectronic package 92..." should read --...microelectronic package array 92....--.

Signed and Sealed this

Twenty-seventh Day of May, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office